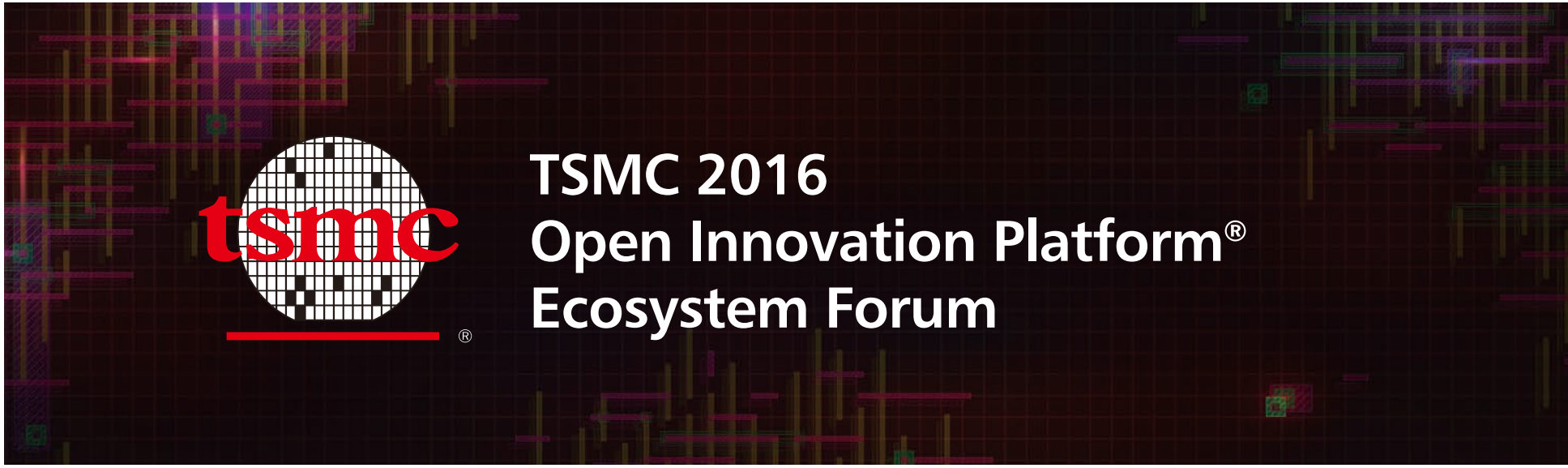
Design & Debug Your TSMC InFO Design Quickly and Accurately

Mentor Graphics



ABSTRACT

TSMC's InFO technology provides for significant improvements in performance, power, and package footprint by combining heterogeneous dies into a single package. Because the InFO approach spans both IC and package design domains, companies need a new design infrastructure that bridges the design gap and integrates the verification needs of both domains. We present new design and verification techniques that improve the manufacturability and reliability of the entire package across multiple die. Attendees will learn how to use the Xpedition® Package Integrator solution for package design and the Calibre® Physical Verification platform for golden sign-off to generate manufacturing-compliant InFO design packages.

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Mentor Graphics

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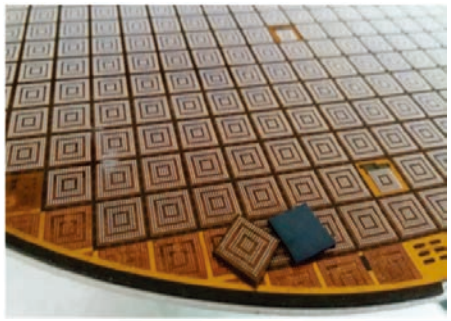
Mentor Graphics

Advantages of InFO Over Conventional Packaging Technologies

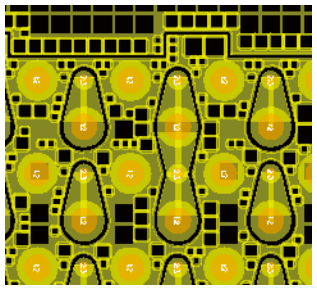
- Higher performance
  - — Shorter interconnect paths
  - — Reduced timing delays
  - — Lower power
  - — Lower thermal resistance
- Improved form-factor
  - — No substrate required
  - — Thinner and lighter
- Lower Cost
  - — No silicon interposer processing



Some Challenges/Considerations for FOWLP

Part "Packaging," Part "Chip Design"

- Operating System
  - — Windows vs. Linux
  - — Layout and Verification on the same environment?
- IC or Packaging technologies?
  - — Silicon RDL layers, Organic RDL layers, Mold/Plastic layers?
  - — Each has their own unique design rules to increase yield
- Manufacturing outputs
  - — GDSII, OBD++, Gerber?
- Netlisting Formats
  - — Spice, Verilog, CSV, AIF, …



Mentor Graphics Flow for TSMC InFO

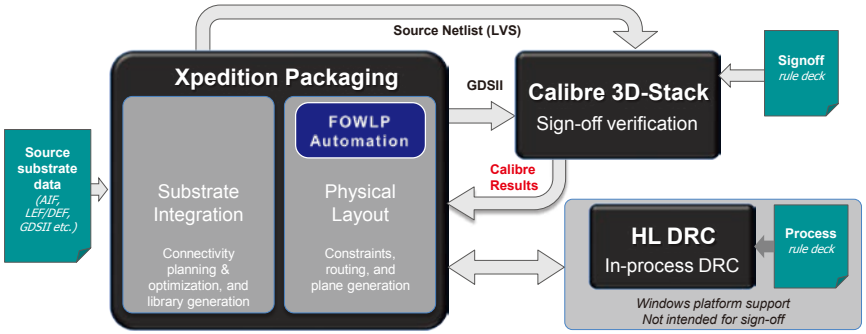
Mentor Graphics Adds Support for Integrated Fan-Out (InFO) Packaging Technology at TSMC

Integration of Calibre and Xpedition Platforms Provides Co-Verification Solution for InFO Design Applications

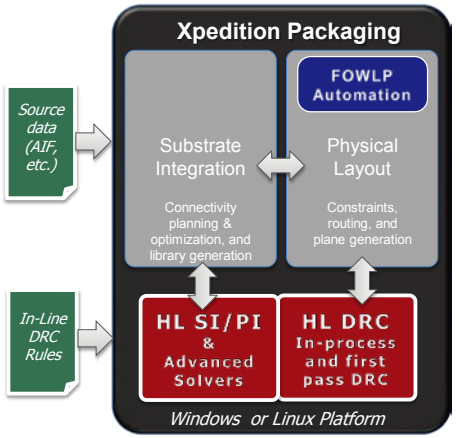
WILSONVILLE, Ore., March 14, 2016— Mentor Graphics Corporation (NASDAQ: MENT) today announced a design, layout, and verification solution to support design applications for TSMC's Integrated Fan-Out (InFO) wafer-level packaging technology. The solution comprises the Calibre® nmDRC physical verification product, the Calibre RVE™ results viewing platform, and the Xpedition® Package Integrator flow. It enables mutual customers to deploy the unique fan-out layer structures and interconnects in the TSMC InFO technology, targeting cost-sensitive applications such as mobile and consumer products.

The interplay between today's advanced system-on-chip (SoC) technologies and packaging requirements is driving the need for co-validation between integrated circuit (IC) and package design environments. The Xpedition Package Integrator flow will be Mentor's platform to support TSMC's unique TSMC InFO design requirements, including integration with other Mentor solutions—the first being Calibre nmDRC and Calibre RVE.

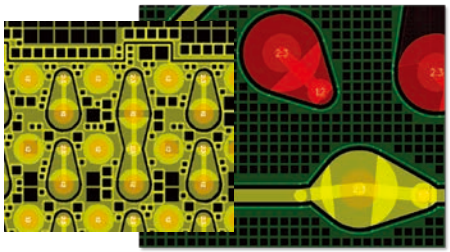
Mentor FO-WLP Co-Design Flow
Complete layout and verification solution



Xpedition FO-WLP Co-Design Platform

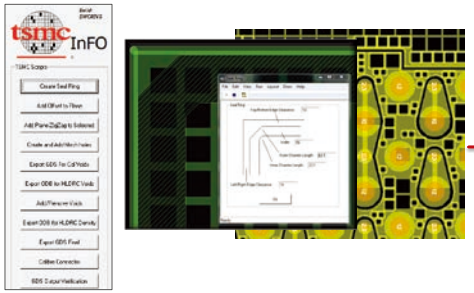


Accuracy & Performance
Predictable Quality Of Results



- ✓ Correct by construction methodology eliminates the costly find & fix approach
- ✓ Complex areafill/planes with accurate representation of the smallest geometries
- ✓ Supports graduated degassing, density & acute angle checks, and stress relief
- ✓ Quality GDSII of non-Manhattan shapes minimizes false verification errors

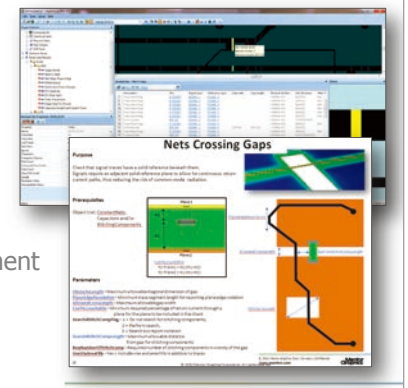
TSMC/Mentor InFO Technology Kit
Specialized functionality in a comprehensive flow



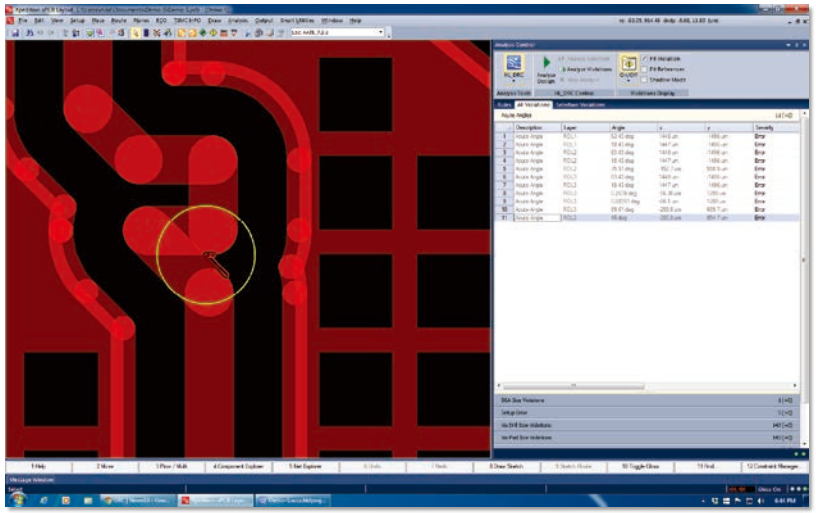
- ✓ InFO-specific PDK and templates
- ✓ Produce the unique geometries necessary for InFO manufacturing
- ✓ Automated stress relief features – mesh pads, zig-zag, graduated degassing…
- ✓ Fast optimized GDS output
- ✓ Comprehensive LVS/LVL/3D verification with Calibre/Xpedition integration

HyperLynx DRC - Electrical Rule Checking

- Design rule checks
  - Automates design checks, eliminating errors from manual inspection and/or in-house developed custom tools and scripts
  - Reduces days of manual design checks to a few hours
- Includes built-in rules
  - Design rule checks for SI, PI
    - Items not quickly/easily simulated
- Allows for rule customization
  - Easily access database objects through automation
  - Advanced geometric operations
  - Script writing/debugging environment



HL-DRC: Improving Designer Productivity



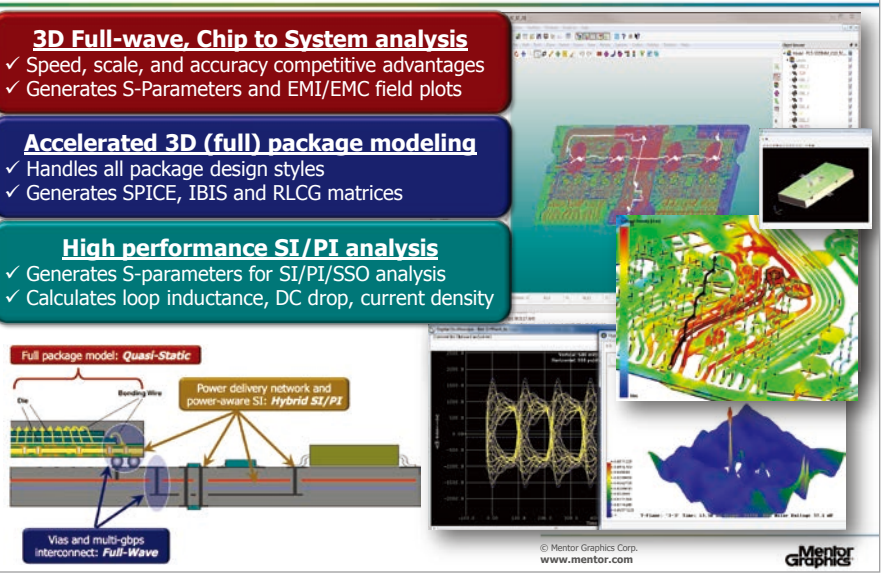
Electrical Modeling & Analysis

Powered by HyperLynx & Nimbic

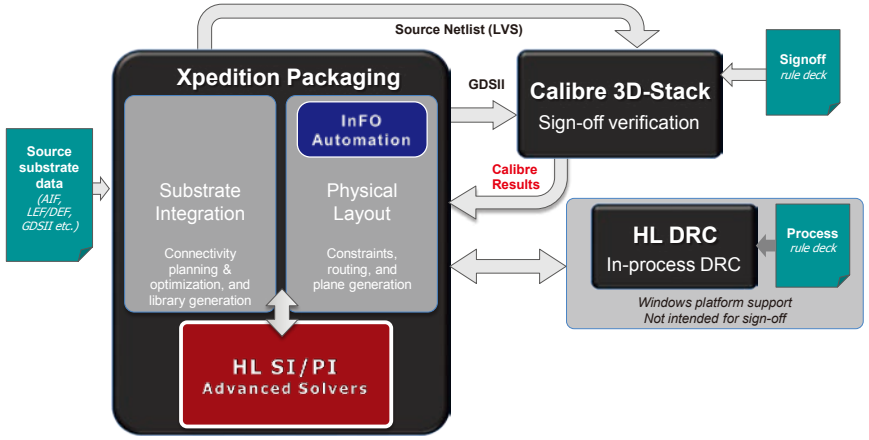
3D Full-wave, Chip to System analysis
- ✓ Speed, scale, and accuracy competitive advantages
- ✓ Generates S-Parameters and EMI/EMC field plots

Accelerated 3D (full) package modeling
- ✓ Handles all package design styles
- ✓ Generates SPICE, IBIS and RLCG matrices

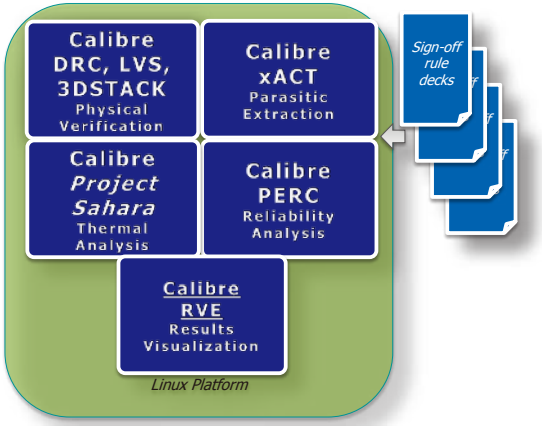
High performance SI/PI analysis
- ✓ Generates S-parameters for SI/PI/SSO analysis
- ✓ Calculates loop inductance, DC drop, current density



Block Diagram of Mentor's InFO Flow

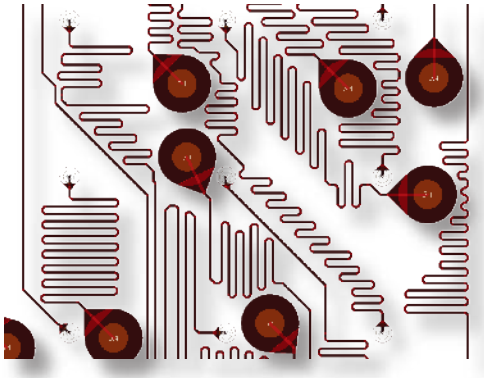


Calibre FO-WLP Verification Platform



InFO Physical Verification Challenges

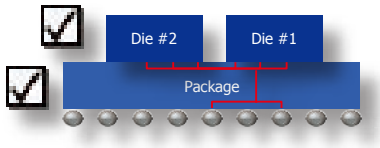
- Multiple Components
  - One or more die
  - Package
  - BGA
  - Substrate
  - …
- Non-Manhattan Shapes
  - Vias, tapers, BGAs, etc.
- Disparate File Standards
  - GDSII vs MCM, ODB++
  - SPICE vs CSV



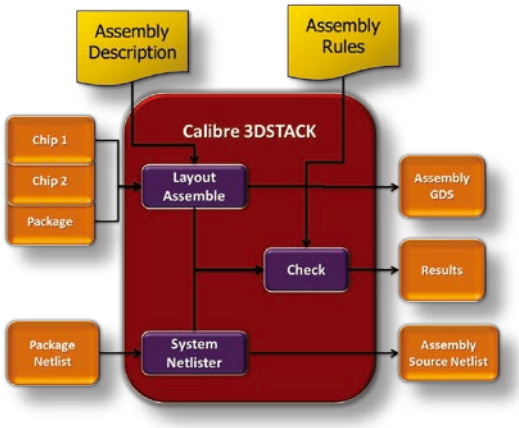
InFO Physical Verification Approach

1. Verify each unique component per process technology

2. Verify interfaces to the package
   - Package geometry DRCs
   - Package geometry to die geometry
   - Connectivity checking from die through package

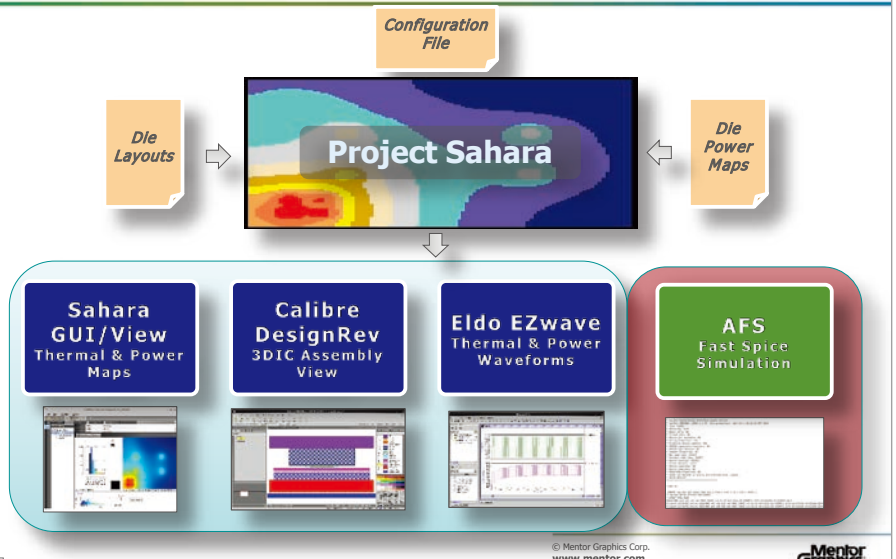


Package Sign-Off: Calibre 3DSTACK

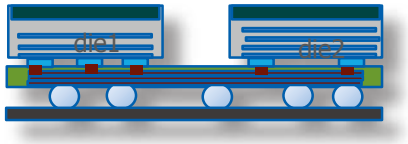


- Manufacturing DRC
  - Package checks
  - Die-Package checks
  - Process independent
  - Curve sensitive
- Signal Integrity
  - CSV, AIF, Spice, Verilog
  - LVS through package
  - Package level PEX

Project Sahara:
Comprehensive Thermal Analysis

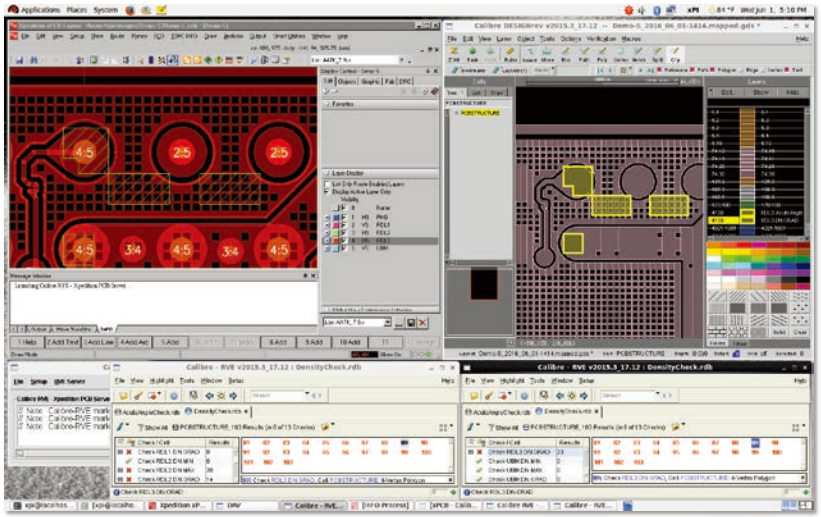


Other On-Going Joint Development: InFO WLP Parasitic Extraction



- Types of Analysis
  - Static Timing Analysis
  - Signal Integrity
  - Power Integrity, …
- Which Parasitics to Extract
  - Analysis of the parasitic impact on design parameters is needed
  - Special attention to die/package (InFO) couplings
    - Capacitive coupling
    - Inductance
- What Kind of Tools to Use?
  - Depends on the required flow, accuracy, performance
  - IC tools for the dies; Package/PCB tools for a InFO package?
    - Good if there is no coupling
    - If there is coupling, choice depends on the flow, accuracy, run time...
- Mentor & TSMC Exploring Multiple Extraction Approaches

Calibre to Xpedition Integration



Summary

- InFO Benefits
  - Footprint
  - Power
  - Performance
  - Costs
- TSMC is Changing the FO-WLP Landscape with InFO
  - Dedicated Reference Flows, Design Kits, Sign-off Methodologies
  - One-stop shopping
- Mentor Graphics Co-Design Flow
  - Xpedition Integration Platform
  - Calibre Verification Platform
  - Unique Design Flow Integration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